IN THE CLAIMS:

Please amend the claims as set forth below:

1. (Currently Amended) A way predictor comprising:

a decoder ~~configured to decode~~ that decodes an indication of a first address that is to access a cache for a current cache access during use, the decoder ~~configured to select~~ selecting a set responsive to the indication of the first address during use;

a memory coupled to the decoder, wherein the memory ~~is configured to output~~ outputs a plurality of values from the set in response to the decoder selecting the set during use, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory, wherein the cache includes a same number of ways as the memory, and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data memory storing the cache lines during use, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache in a respective way of the plurality of ways and in the set; and

a circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the circuit ~~is configured to compare~~ compares the first value to the plurality of values during use, and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the circuit to predict the first way to be a hit in the cache for the first address for the current access during use, and wherein the circuit ~~is configured to output~~ outputs a way identifier identifying the first way to the data memory during use, the way identifier used by the data memory to select the first way to output data during use, and wherein the circuit ~~is~~

~~configured to construct~~ constructs the way identifier based on the comparisons of the first value to the plurality of values during use.

2. (Cancelled)

3. (Currently Amended) The way predictor as recited in claim 1 wherein the circuit, if none of the plurality of values matches the first value, ~~is configured to assert~~ asserts an early miss signal during use.

4. (Original) The way predictor as recited in claim 1 wherein each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag.

5. (Original) The way predictor as recited in claim 1 wherein each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line.

6. (Original) The way predictor as recited in claim 5 wherein each of the plurality of values comprises a portion of one or more address operands used to generate the address.

7. (Original) The way predictor as recited in claim 5 wherein at least one bit of one of the plurality of values is a logical combination of two or more bits of the address.

8. (Original) The way predictor as recited in claim 5 wherein at least one bit of one of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address.

9. (Original) The way predictor as recited in claim 1 wherein the indication of the first address comprises at least a portion of the first address.

10. (Previously Presented) The way predictor as recited in claim 1 wherein the indication

of the first address comprises two or more address operands used to generate the first address.

11. (Currently Amended) The way predictor as recited in claim 1 wherein, if the first way is an incorrect prediction, the cache ~~is configured to replace~~ replaces a cache line in the first way with a missing cache line corresponding to the first address during use.

12. (Currently Amended) The way predictor as recited in claim 11 wherein, if no way prediction is generated and a cache miss results for the first address, the cache ~~is configured to use~~ uses a replacement algorithm to select the cache line to be replaced with the missing cache line during use.

13. (Currently Amended) A method comprising:

decoding an indication of a first address that is to access a cache to select a set;

outputting a plurality of values from the set in a memory in response to the set being selected, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory, wherein the cache includes a same number of ways as the memory, and wherein the cache includes a tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data memory storing the cache lines, and wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line stored in the cache in a respective way of the plurality of ways and in the set;

comparing each of the plurality of values to ~~the~~ a first value corresponding to the first address, and wherein a hit in a first way of the cache is indicated for prediction based on a match of the first value and a second value stored in the first way of the memory;

predicting the first way of the plurality of ways to be a hit in the cache for the first address responsive to the first value matching one of the plurality of values; and

constructing a way identifier that identifies the first way to the data memory, the way identifier used by the data memory to select the first way to output data, and wherein the constructing is based on the comparisons of the first value to the plurality of values.

14. (Cancelled)

15. (Previously Presented) The method as recited in claim 13 further comprising, if none of the plurality of values matches the first value, indicating a miss.

16. (Original) The method as recited in claim 13 wherein each of the plurality of values comprises a portion of a tag identifying a corresponding cache line in the cache, the portion excluding at least one bit of the tag.

17. (Original) The method as recited in claim 13 wherein each of the plurality of values is derived from at least a portion of the indication of the address identifying a corresponding cache line.

18. (Original) The method as recited in claim 17 wherein each of the plurality of values comprises a portion of one or more address operands used to generate the address.

19. (Original) The method as recited in claim 17 wherein a bit of each of the plurality of values is a logical combination of two or more bits of the address.

20. (Original) The method as recited in claim 17 wherein a bit of each of the plurality of values is a logical combination of two or more bits of one or more address operands used to generate the address.

21. (Previously Presented) The method as recited in claim 13 further comprising:

detecting that the first way is an incorrect prediction; and

replacing a cache line in the cache in the first way with a missing cache line corresponding to the first address.

22. (Original) The method as recited in claim 21 further comprising, if no way prediction is generated and a cache miss results for the first address, using a replacement algorithm to select the cache line to be replaced with the missing cache line.

23. (Currently Amended) An apparatus comprising:

a way predictor comprising:

a decoder ~~configured to decode~~ that decodes an indication of a first address that is to access a cache for a current cache access during use, the decoder ~~configured to select~~ selecting a set responsive to the indication of the first address during use;

a memory coupled to the decoder, wherein the memory ~~is configured to output~~ outputs a plurality of values from the set in response to the decoder selecting the set during use, wherein each of the plurality of values corresponds to a different way of a plurality of ways of the memory, wherein the cache includes a same number of ways as the memory, and wherein the cache includes a data cache tag memory storing a plurality of tags corresponding to cache lines stored in the cache and a data cache data memory storing the cache lines during use, wherein each of the plurality of values comprises a plurality of bits associated with a corresponding cache line in the

cache in a respective way of the plurality of ways and in the set; and

a first circuit coupled to receive the plurality of values and a first value corresponding to the first address, wherein the first circuit ~~is configured to compare~~ compares the first value to the plurality of values during use, and wherein a match of the first value and a second value stored in a first way of the plurality of ways causes the first circuit to predict the first way to be a hit in the cache for the first address for the current access during use, and wherein the first circuit ~~is configured to output~~ outputs a way identifier identifying the first way to the data cache data memory during use, the way identifier used by the data cache data memory to select the first way to output data during use, and wherein the first circuit ~~is configured to construct~~ constructs the way identifier based on the comparisons of the first value to the plurality of values during use; and

the data cache data memory coupled to the way predictor, wherein the data cache data memory is arranged into the plurality of ways, and wherein the data cache data memory ~~is configured to output~~ outputs data from the first way during use, and wherein the data cache data memory includes a second circuit ~~configured to reduce~~ that reduces power consumption attributable to one or more non-predicted ways of the plurality of ways during use.

24. (Currently Amended) The apparatus as recited in claim 23 further comprising the data cache tag memory ~~configured to output~~ outputting a tag from the first way and ~~to not output~~ not outputting tags from the one or more non-predicted ways during use.

25. (Currently Amended) The apparatus as recited in claim 23 wherein the second circuit ~~is configured to generate~~ generates separate wordlines for each of the plurality of ways in

the data cache data memory during use, and wherein the second circuit ~~is configured to activate~~ activates a first wordline to the first way and ~~to not~~ does not activate word lines to the non-predicted ways during use.

26. (Currently Amended) The apparatus as recited in claim 25 wherein the second circuit includes column multiplexor circuitry coupled to the plurality of ways, wherein the column multiplexor circuitry selects ~~and configured to select~~ the output of the first way as input to a sense amplifier circuit during use, wherein the column multiplexor circuitry is controlled by the predicted first way.

27. (Currently Amended) The apparatus as recited in claim 23 wherein the second circuit includes column multiplexor circuitry coupled to the plurality of ways, wherein the column multiplexor circuitry selects ~~and configured to select~~ the output of the first way as input to a sense amplifier circuit during use, wherein the column multiplexor circuitry is controlled by the predicted first way.

28. (Previously Presented) The apparatus as recited in claim 23 wherein the second circuit comprises a plurality of sense amplifier circuits, wherein each of the plurality of sense amplifier circuits is coupled to a respective one of the plurality of ways, and wherein each of the plurality of sense amplifier circuits includes an enable input that is controlled by the predicted first way.

29. (Currently Amended) The apparatus as recited in claim 23 further comprising a second level cache, and wherein the circuit ~~is configured to detect~~ detects a miss responsive to the plurality of values and the first value prior to the miss being detected in the cache that corresponds to the data cache data memory during use, and wherein the circuit ~~is configured to signal~~ signals the miss to the second level cache during use, and wherein the second level cache ~~is configured to begin~~ begins an access corresponding to the first address responsive to signal from the circuit during use.